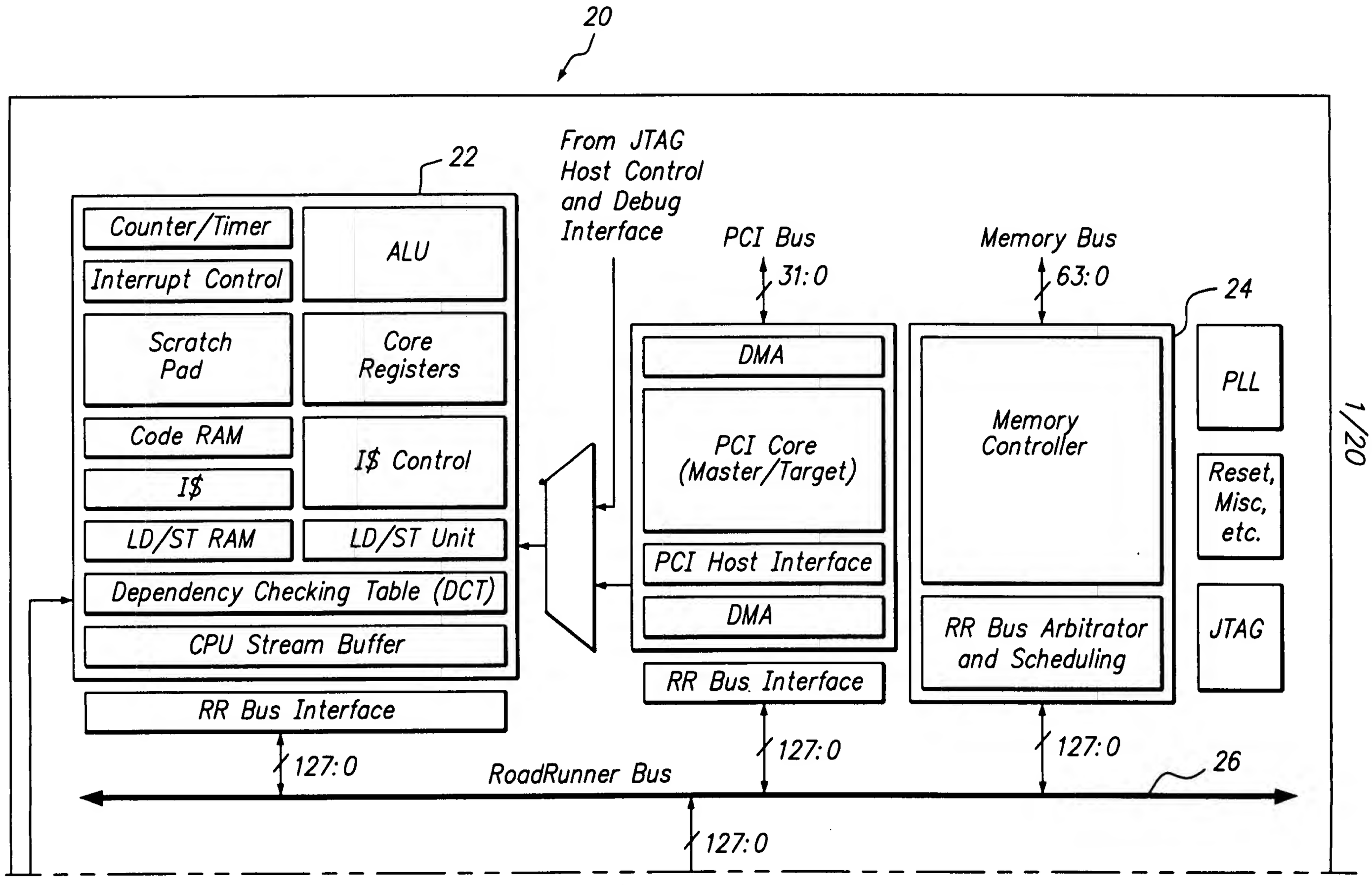


FIG. 1A

Copy

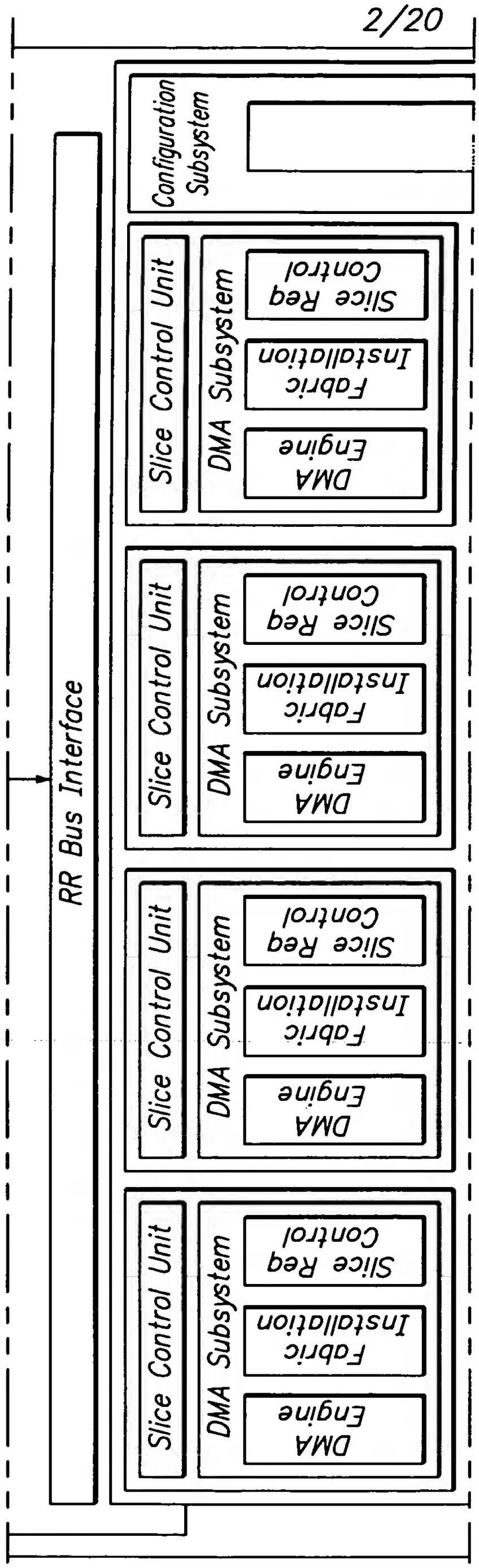


FIG. 1B

FIG. 1

FIG. 1A	FIG. 1B	FIG. 1C

Appln. Filing Date: September 19, 200
Title: Despreader/Correlator Unit for Use in Reconfigurable Chip
Inventor: Bradley L. Taylor, et al.
Application Serial No: 09/960,710

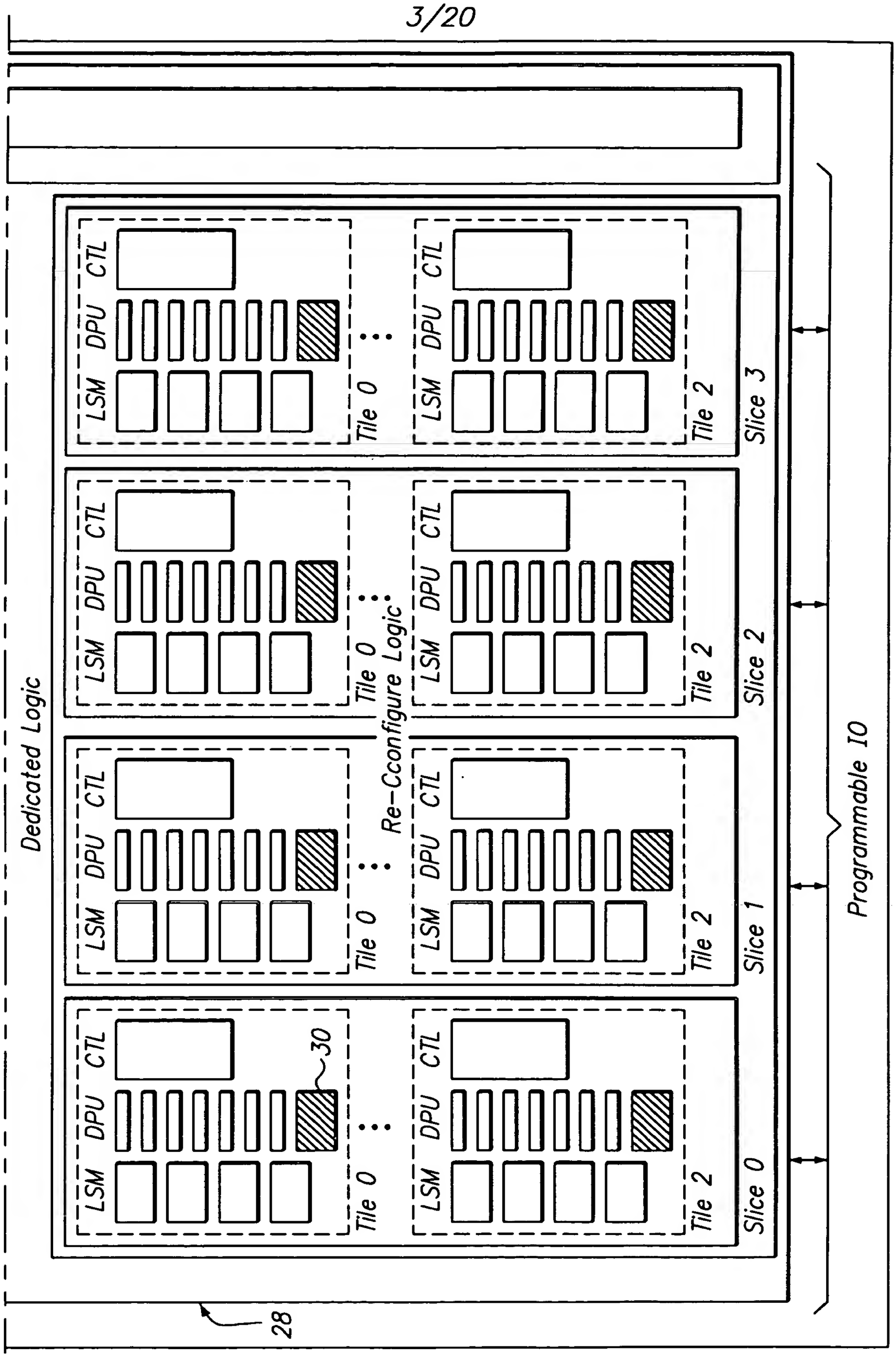


FIG. 1C

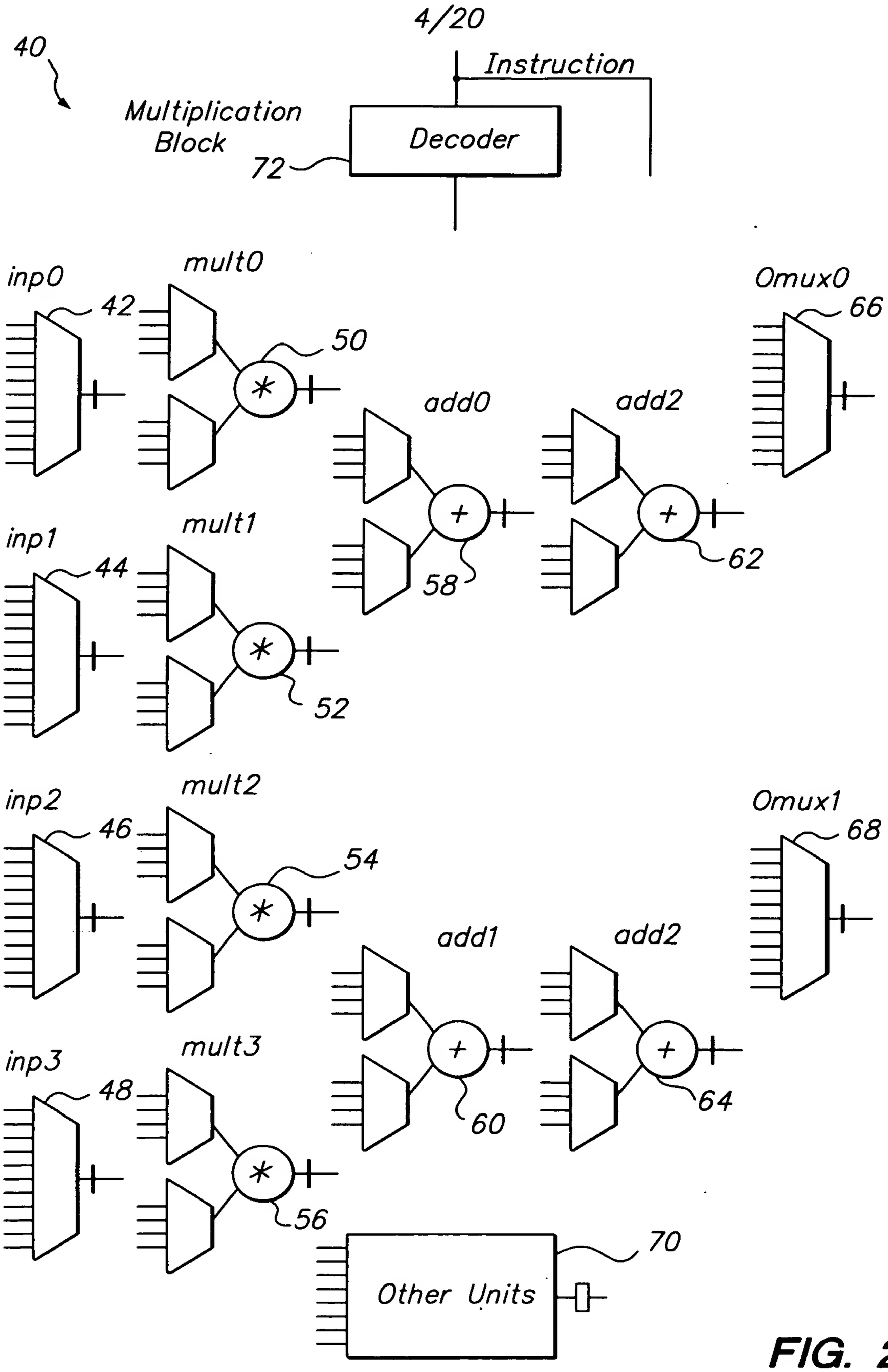

4/20
40
Instruction
Multiplication Block
Decoder
72
inp0
mult0
42
50
Omux0
66
add0
add2
inp1
mult1
44
58
62
inp2
mult2
46
54
add1
Omux1
68
inp3
mult3
48
60
64
56
Other Units
70

FIG. 2

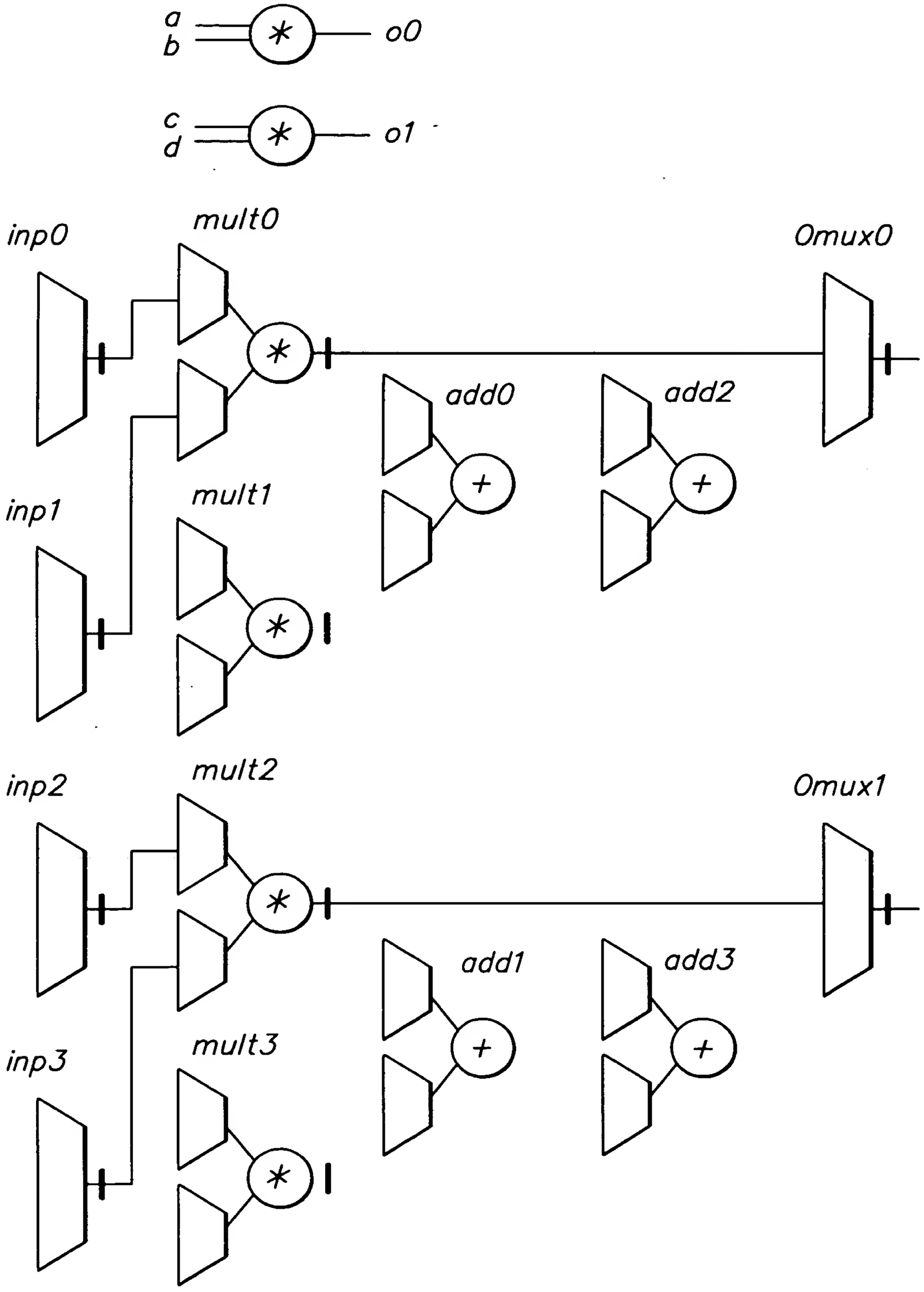

2MULT–CS2112 Compatible mode 2 independent multipliers
a
b
o0
c
d
o1
inp0
mult0
Omux0
add0
add2
inp1
mult1
inp2
mult2
Omux1
add1
add3
inp3
mult3

FIG. 3A

4ADD32–Sum of 4 32–bit inputs

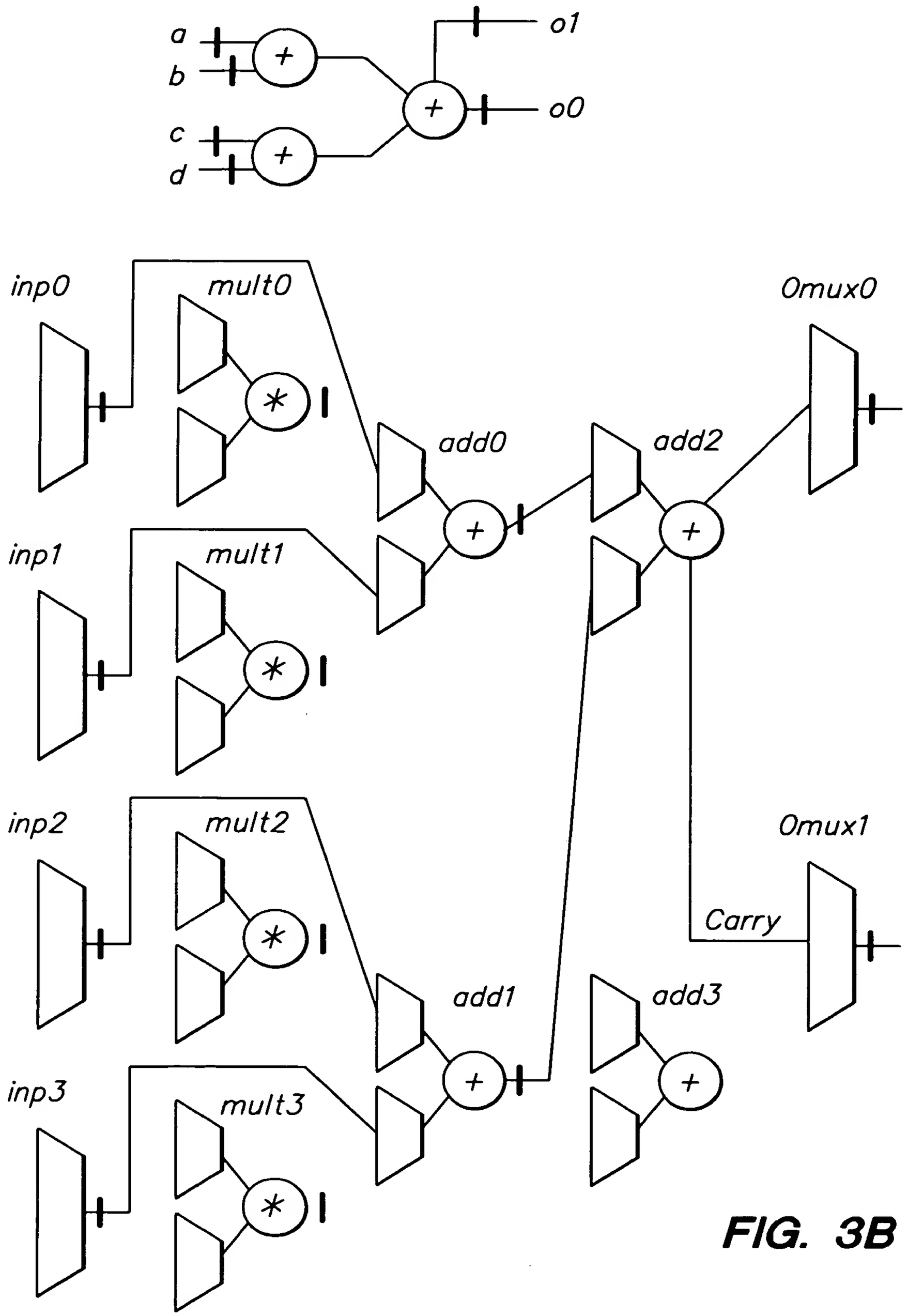
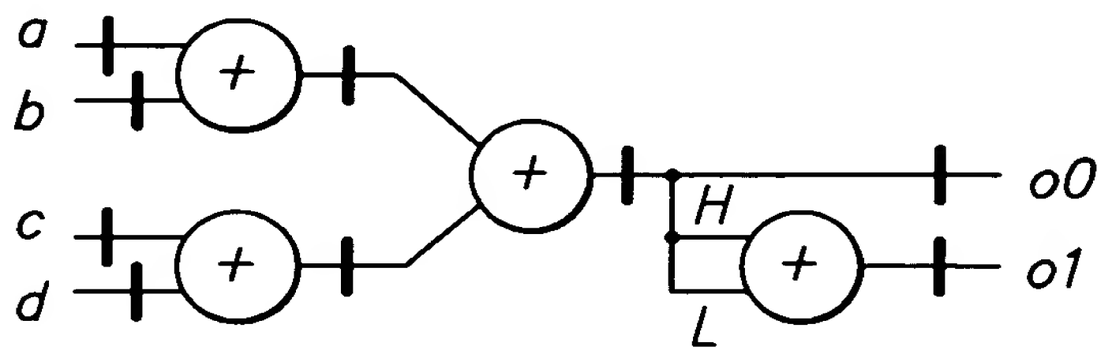


FIG. 3B

4ADD16–Sum of 4 packed 16–bit inputs, sum of upper, lower 16–bits



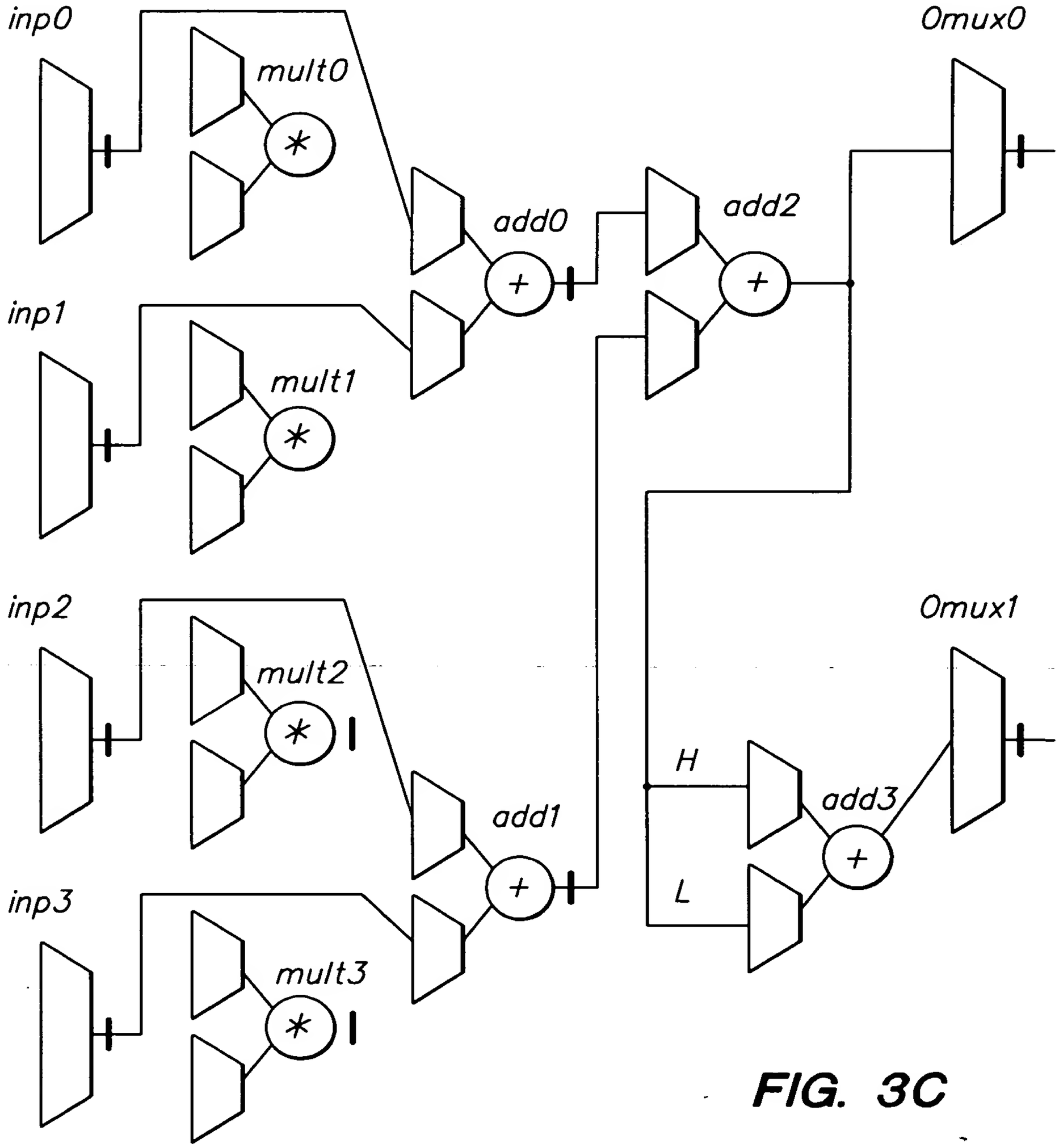


FIG. 3C

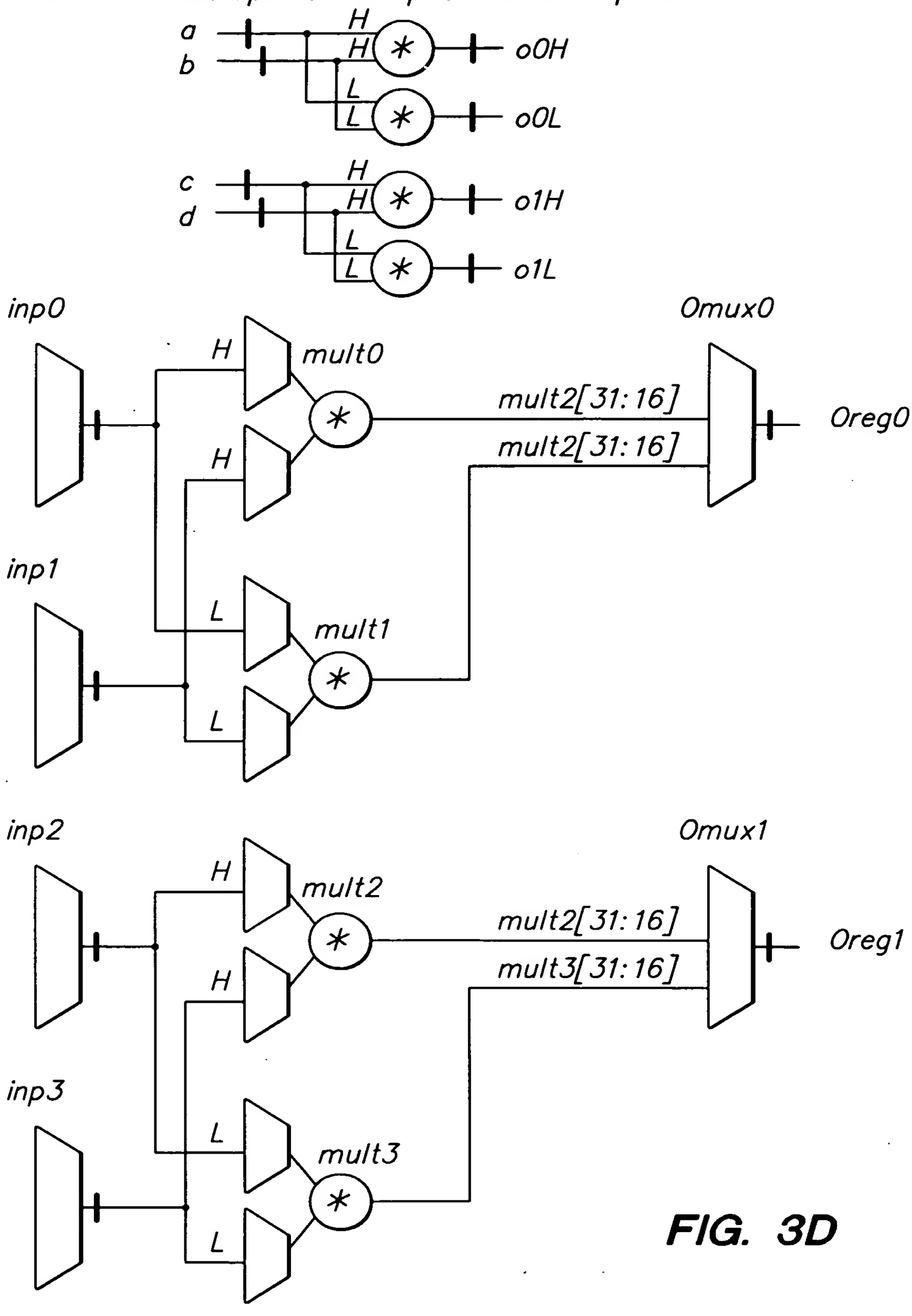

4MULT–4 multipliers with pack 16–bit inputs
a
b
c
d
H
L
*
o0H
o0L
o1H
o1L
inp0
inp1
inp2
inp3
mult0
mult1
mult2
mult3
mult2[31:16]
mult3[31:16]
Omux0
Omux1
Oreg0
Oreg1

FIG. 3D

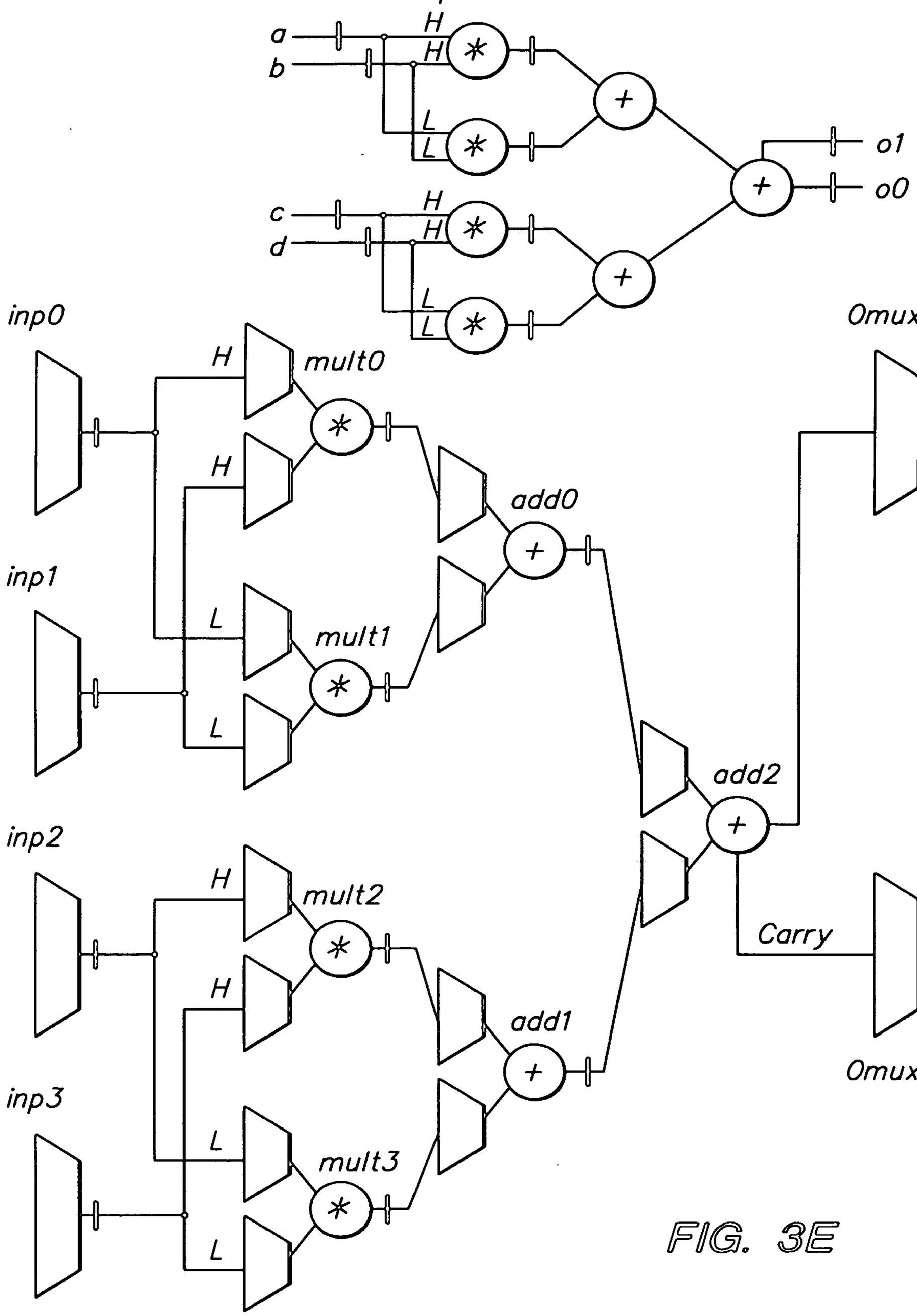

4MULTSUM–Sum of 4 multipliers
a
b
c
d
H
L
*
+
o1
o0
inp0
inp1
inp2
inp3
mult0
mult1
mult2
mult3
add0
add1
add2
0mux0
0mux1
Carry

FIG. 3E

4MULT2SUM–2 Sums of 2 multipliers

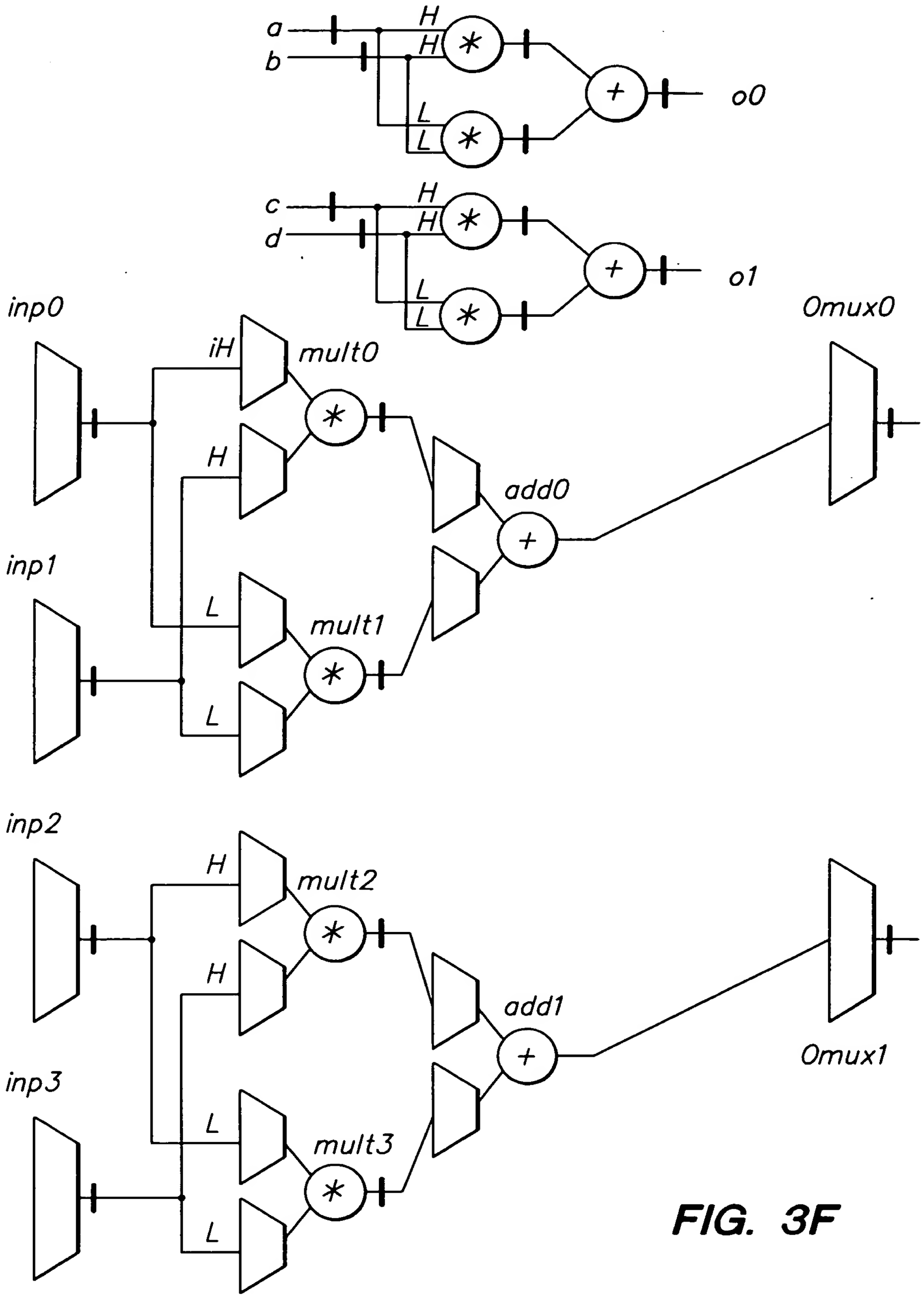


FIG. 3F

CMULT–32–bit output complex multiply with 32–Bit accumulation input, Assumes real part in High 16–bits, imaginary in Low 16–bits

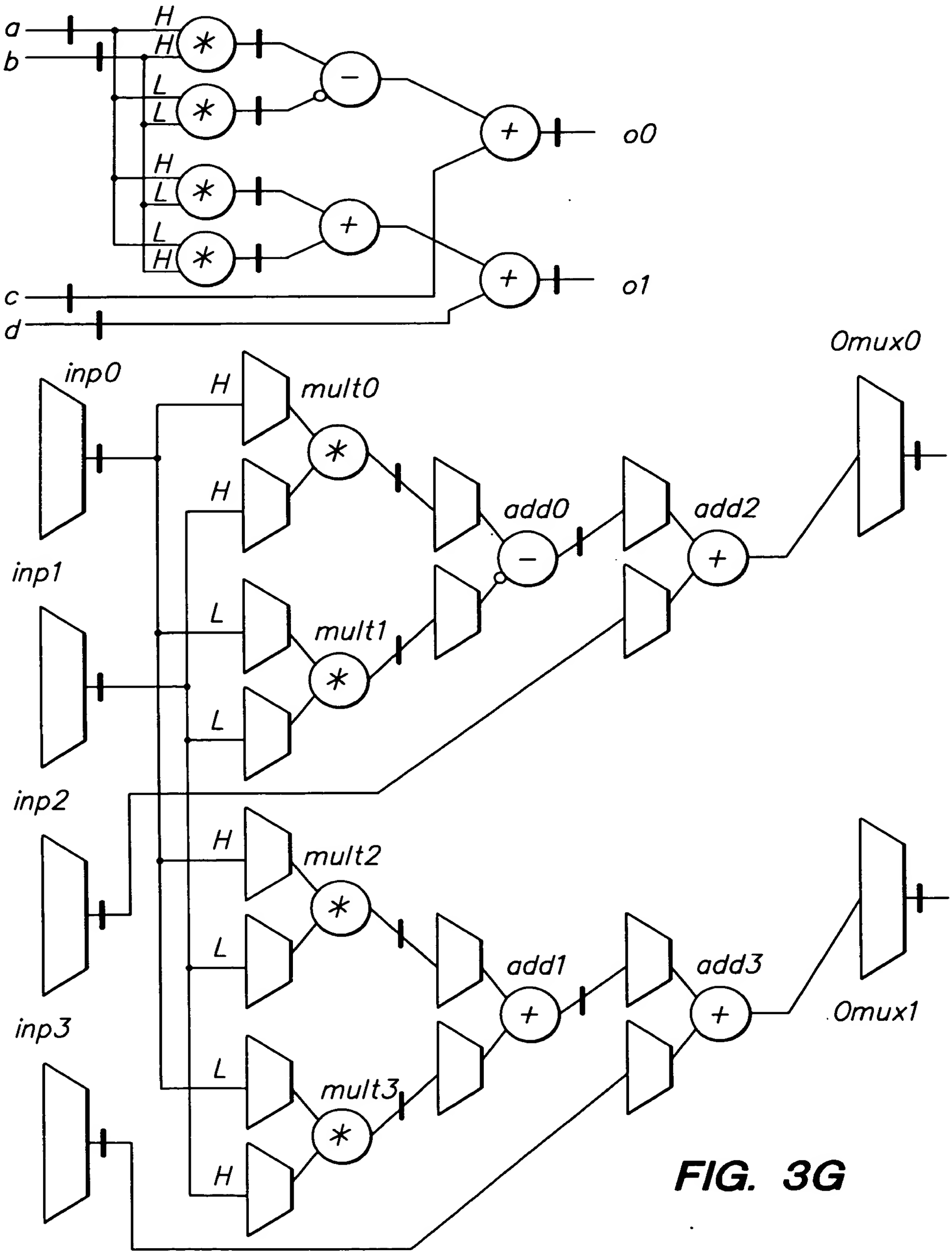


FIG. 3G

CMULT16–Complex Multiplier with 16–Bit Packed data, and indepent delay path. Assumes real part in High 16–bits, imaginary in Low 16–bits

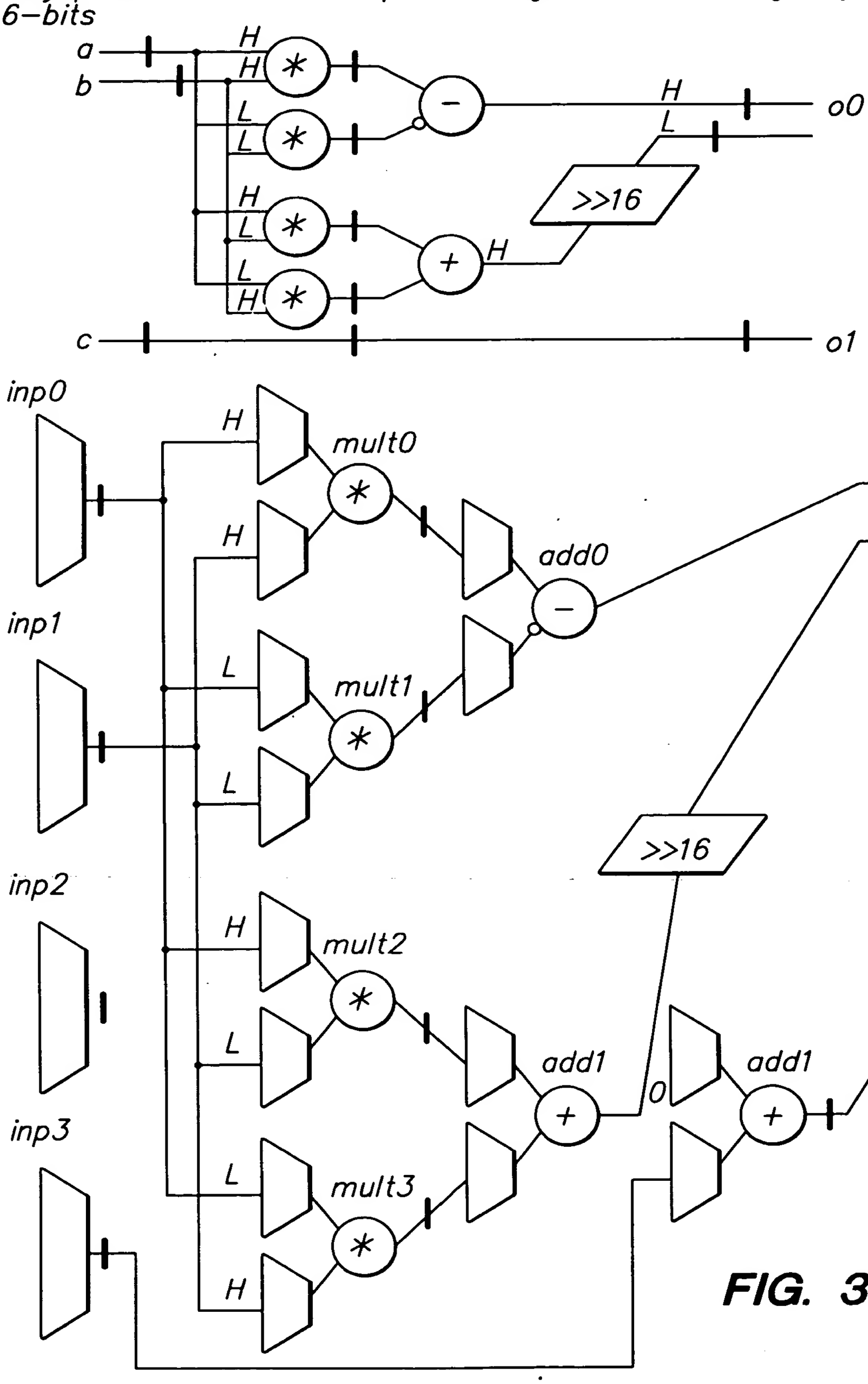
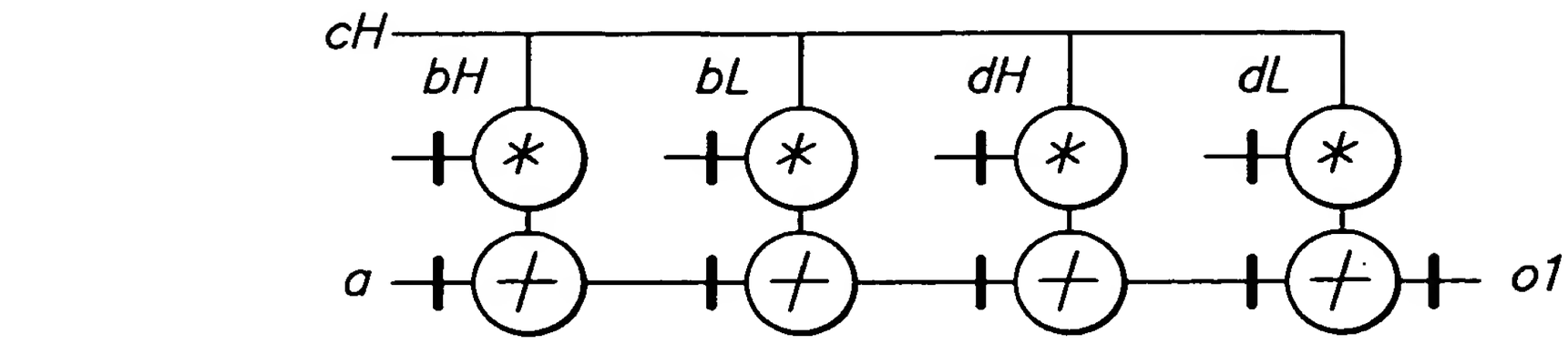


FIG. 3H

4FIR–4 tap FIR filter



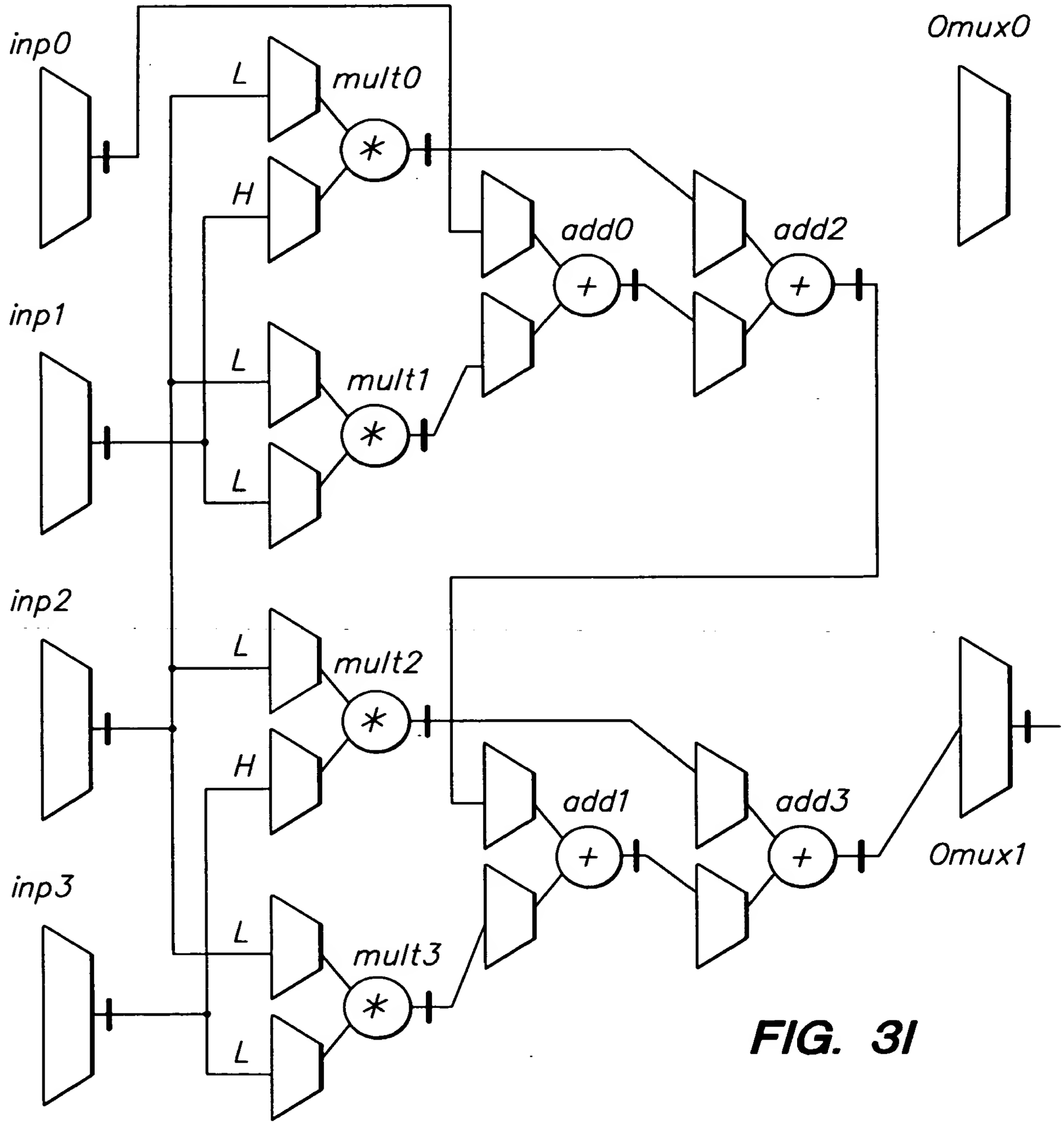


FIG. 3I

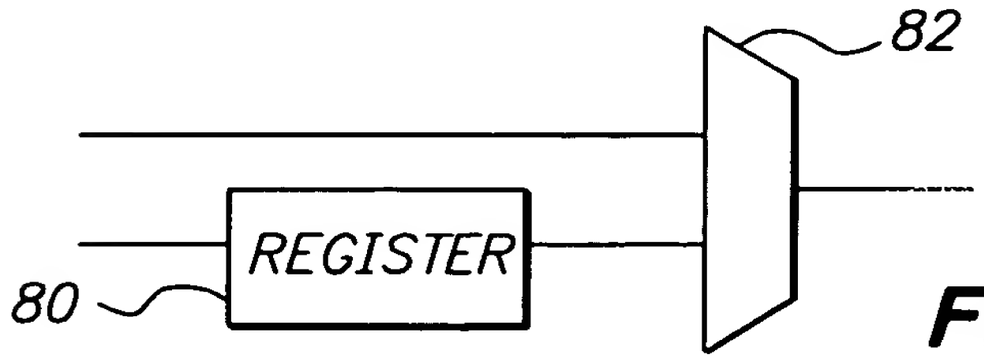


FIG. 4

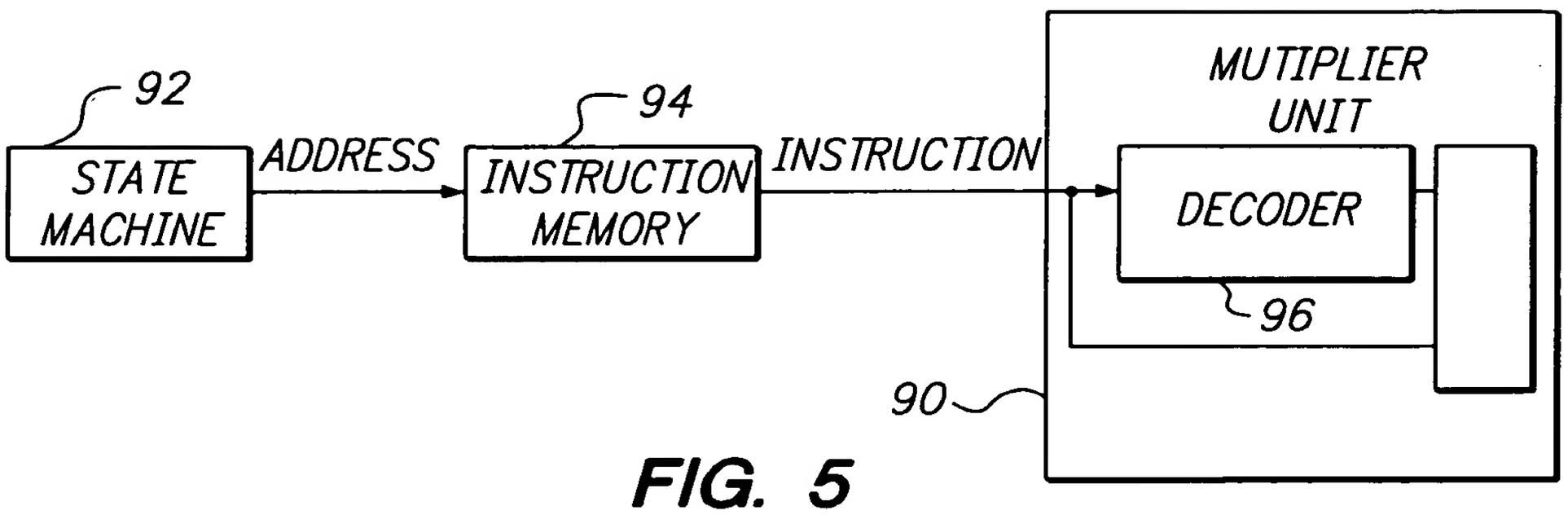


FIG. 5

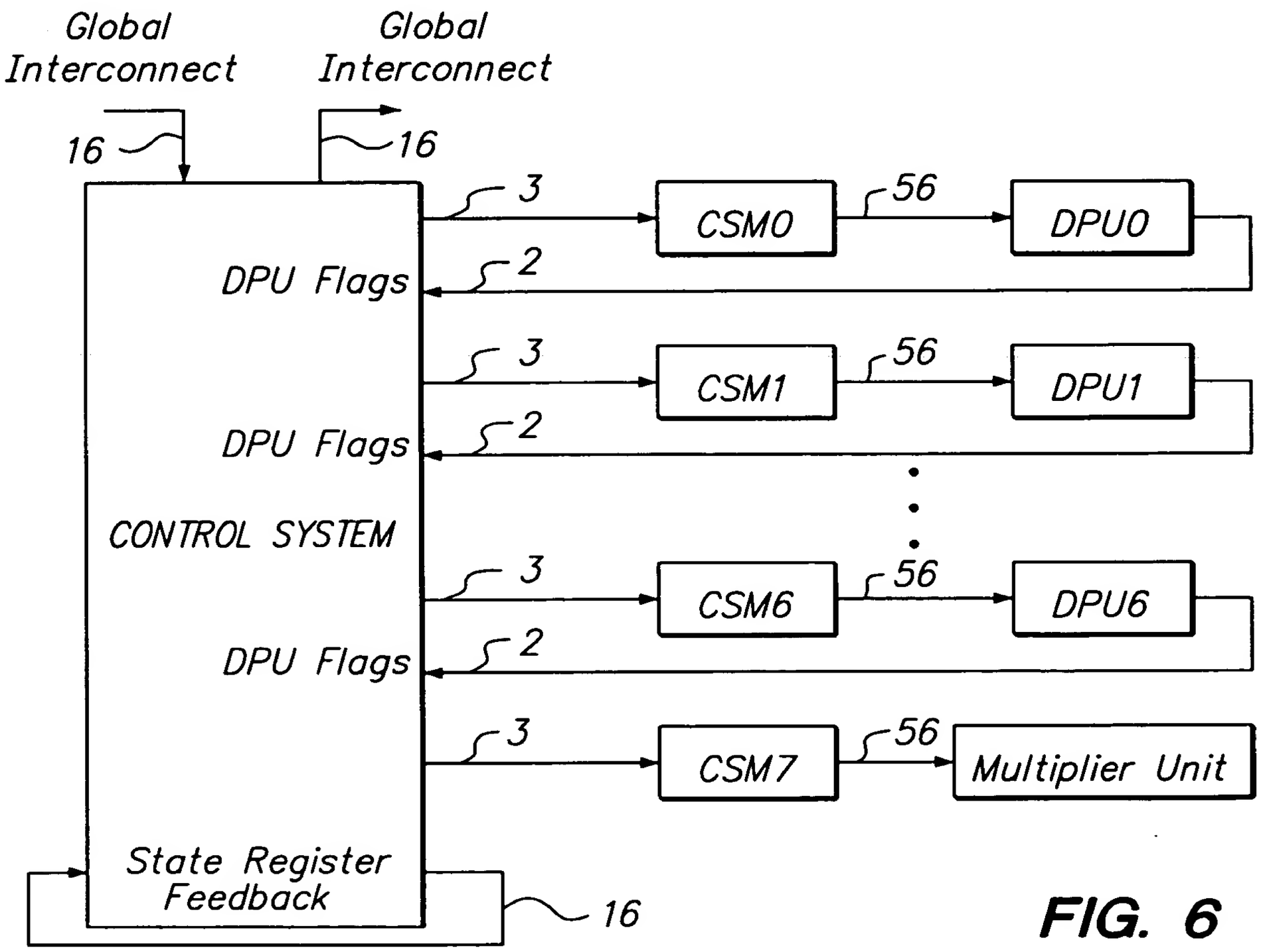


FIG. 6

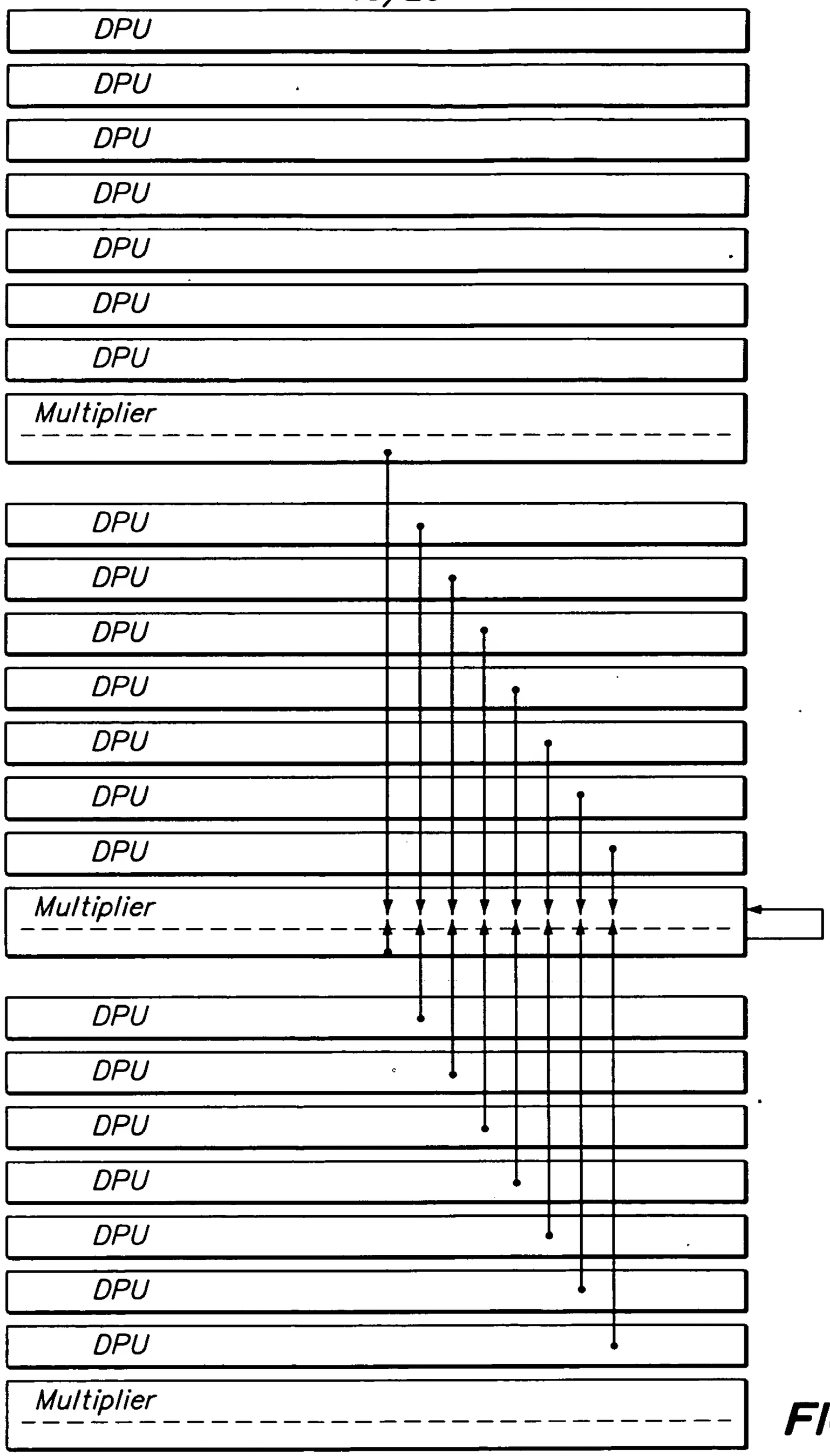

DPU
DPU
DPU
DPU
DPU
DPU
DPU
Multiplier
DPU
DPU
DPU
DPU
DPU
DPU
DPU
Multiplier
DPU
DPU
DPU
DPU
DPU
DPU
DPU
Multiplier

FIG. 7

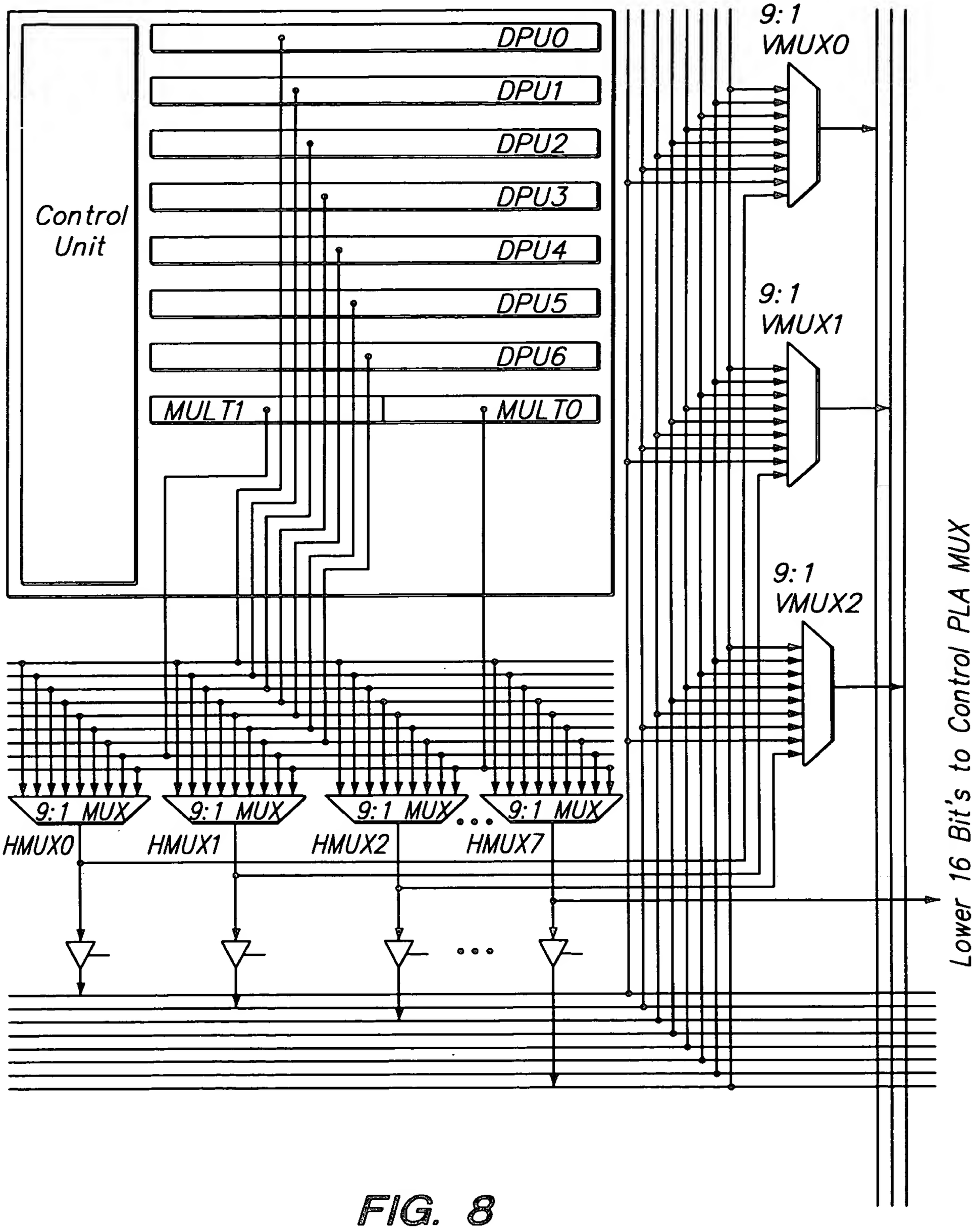

Control Unit
DPU0
DPU1
DPU2
DPU3
DPU4
DPU5
DPU6
MULT1
MULT0
9:1 VMUX0
9:1 VMUX1
9:1 VMUX2
9:1 MUX
HMUX0
HMUX1
HMUX2
HMUX7
Lower 16 Bit's to Control PLA MUX

FIG. 8

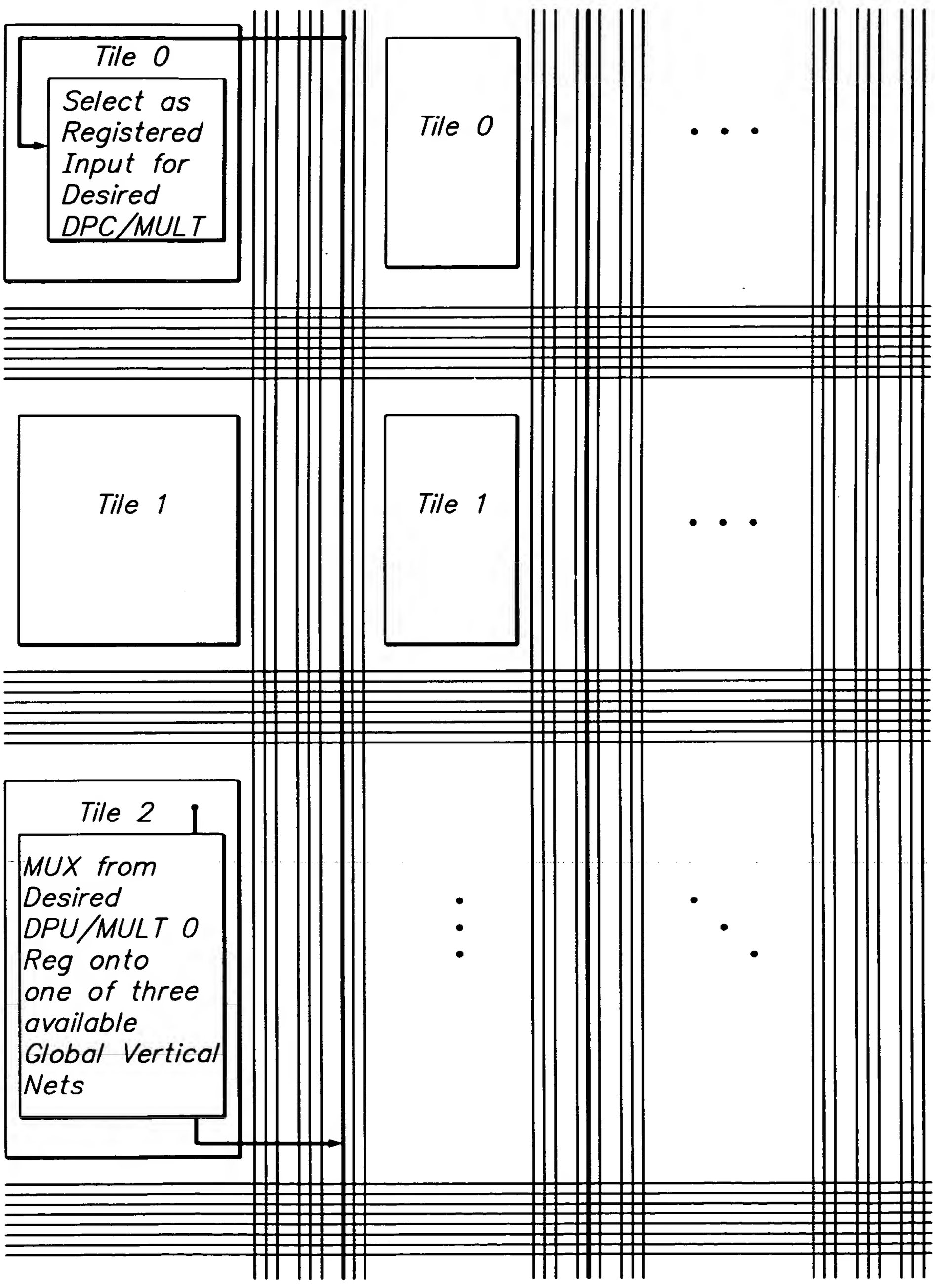

Tile 0
Select as Registered Input for Desired DPC/MULT
Tile 0
Tile 1
Tile 1
Tile 2
MUX from Desired DPU/MULT 0 Reg onto one of three available Global Vertical Nets

FIG. 9

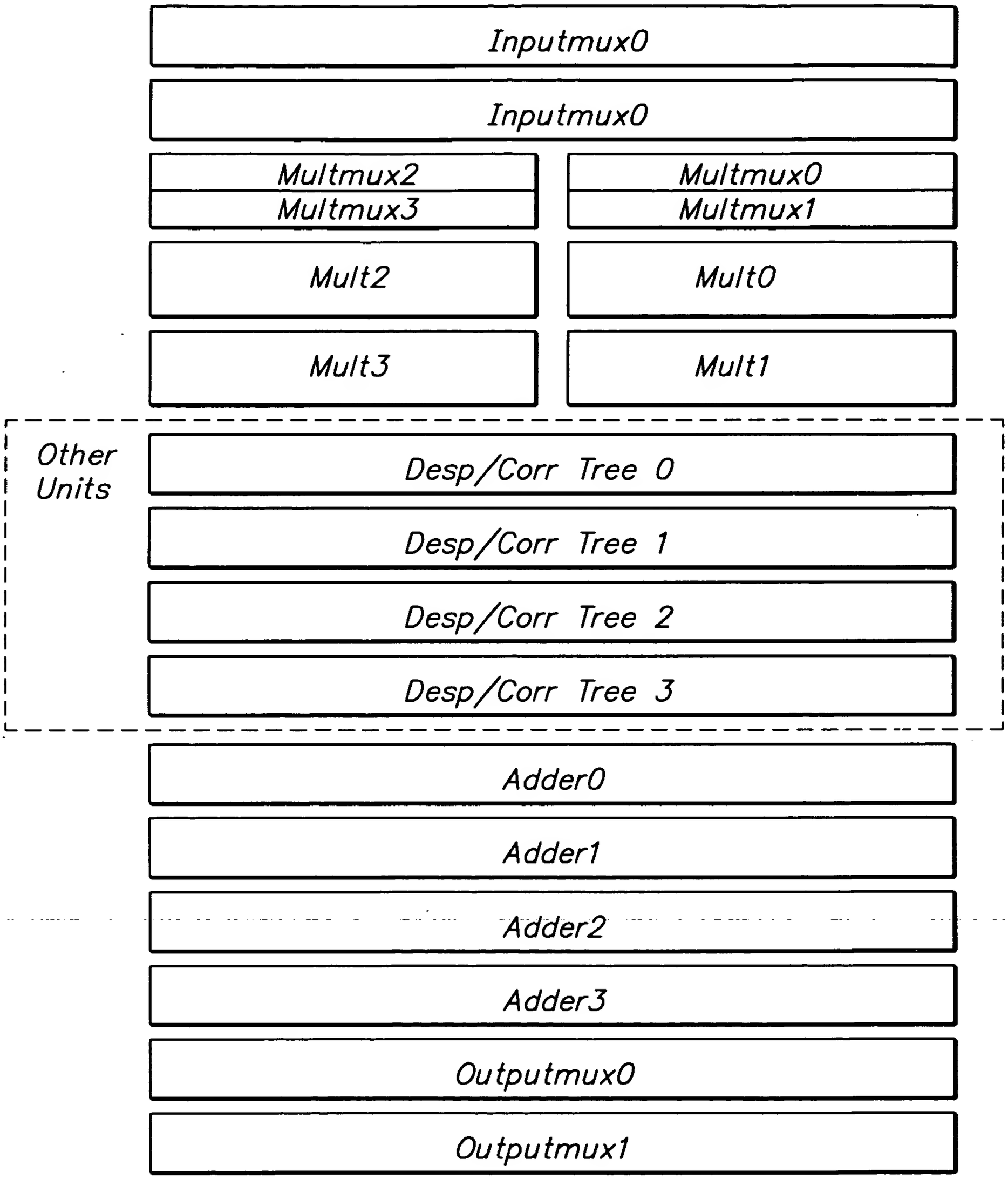

Inputmux0
Inputmux0
Multmux2
Multmux3
Multmux0
Multmux1
Mult2
Mult0
Mult3
Mult1
Other Units
Desp/Corr Tree 0
Desp/Corr Tree 1
Desp/Corr Tree 2
Desp/Corr Tree 3
Adder0
Adder1
Adder2
Adder3
Outputmux0
Outputmux1

FIG. 10

Appln. Filing Date: September 19, 2001
Title: Despreader/Correlator Unit for Use in Reconfigurable Chip
Inventor: Bradley L. Taylor, et al.
Application Serial No: 09/960,710

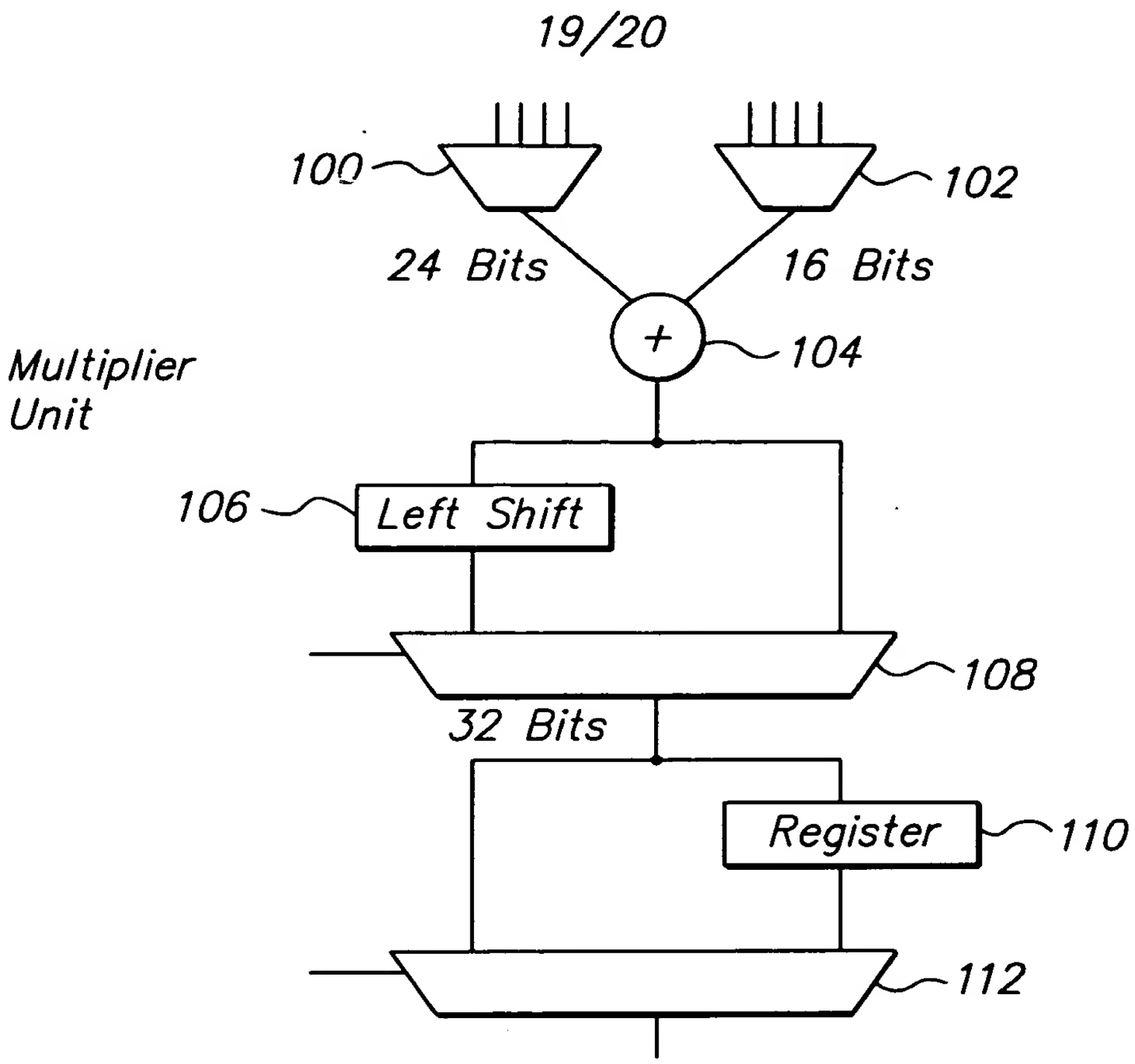


FIG. 11

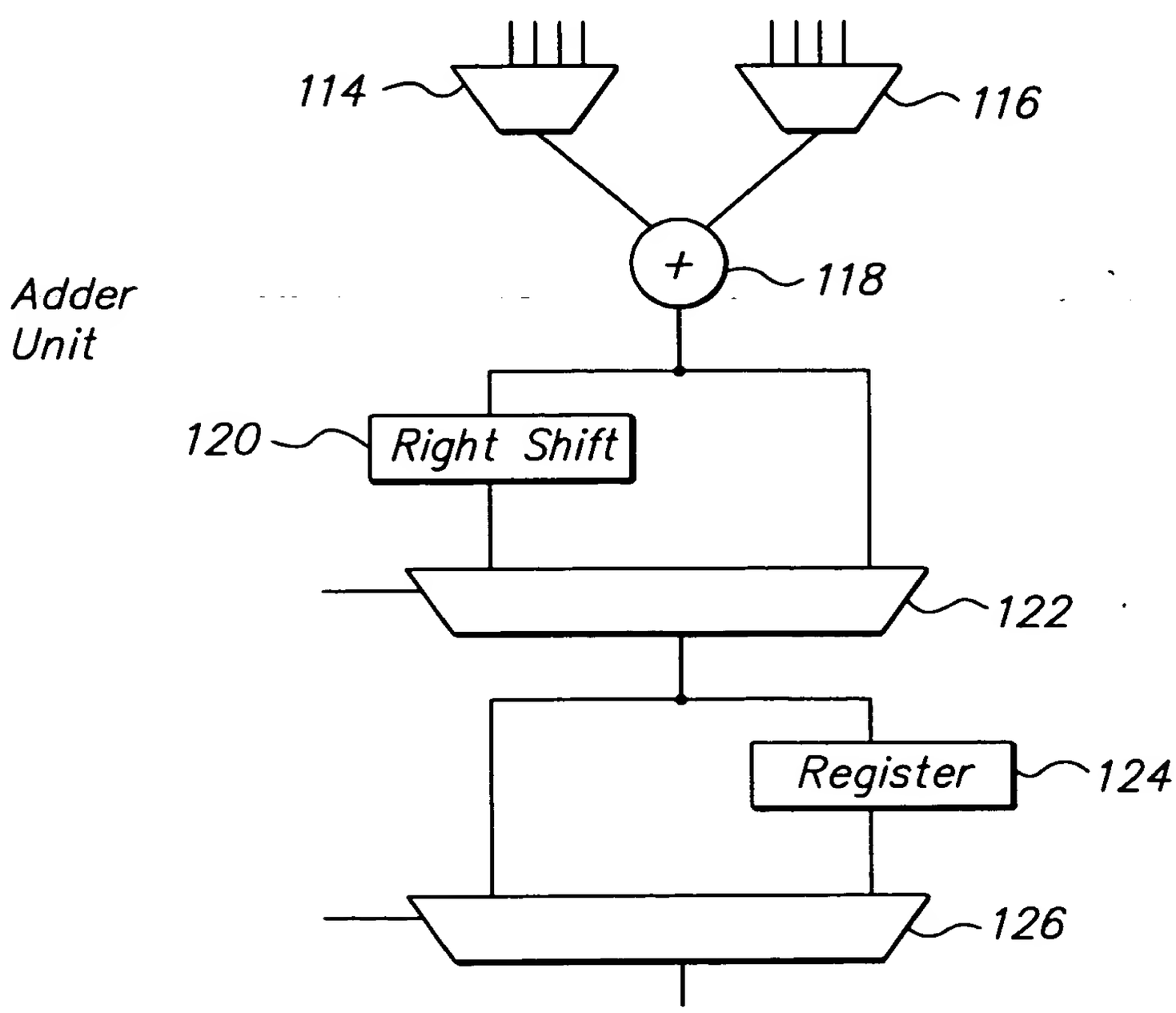


FIG. 12

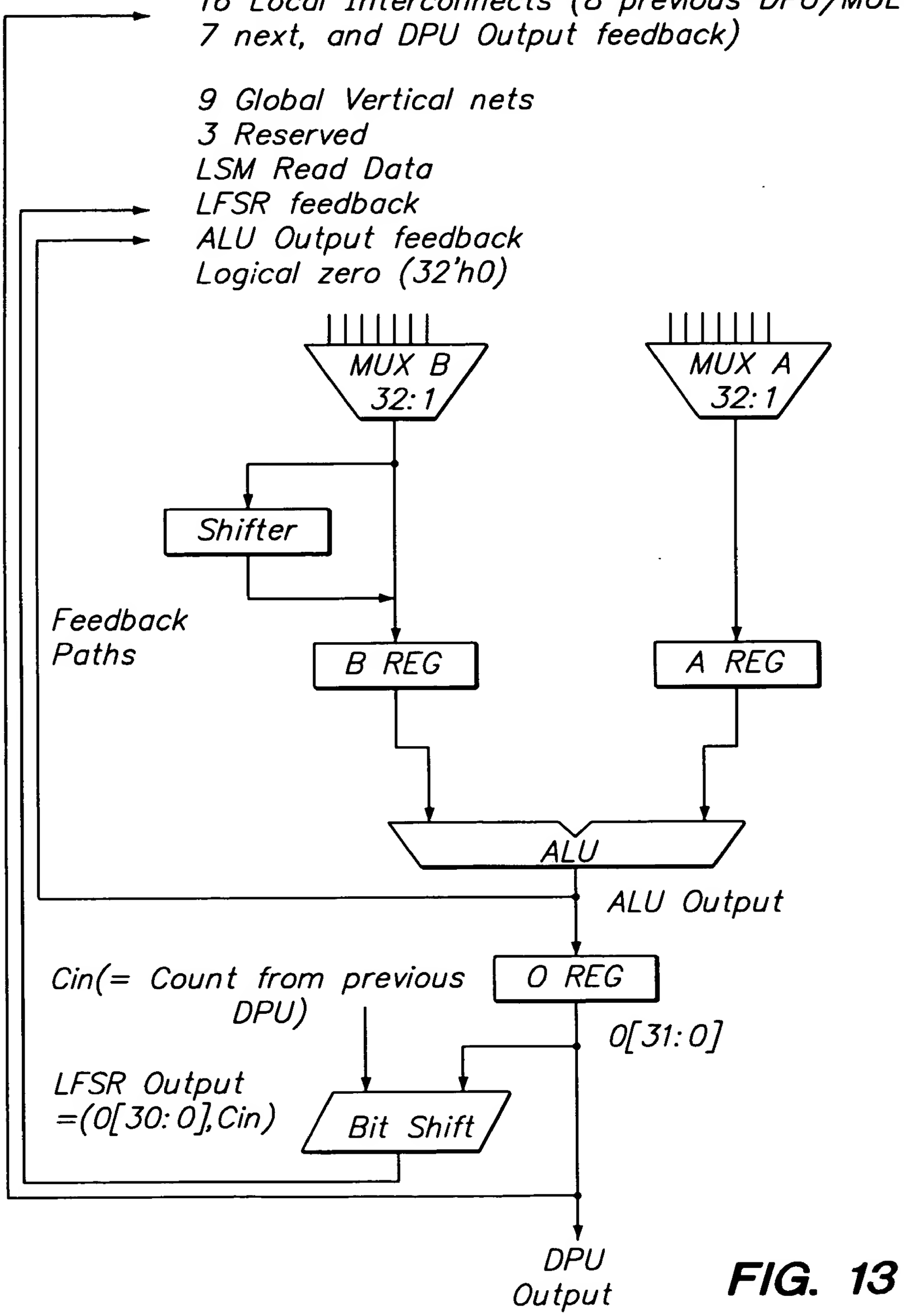

The A and B input muxes select from the following sets of 32-bit signals:
16 Local Interconnects (8 previous DPU/MULTs, 7 next, and DPU Output feedback)
9 Global Vertical nets
3 Reserved
LSM Read Data
LFSR feedback
ALU Output feedback
Logical zero (32'h0)
MUX B 32:1
MUX A 32:1
Shifter
Feedback Paths
B REG
A REG
ALU
ALU Output
O REG
O[31:0]
Cin(= Count from previous DPU)
LFSR Output =(O[30:0],Cin)
Bit Shift
DPU Output

FIG. 13